TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOS III)

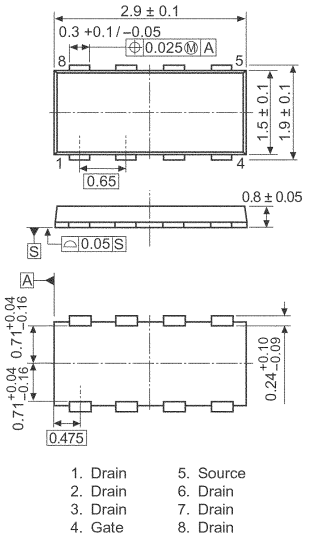
TPCF8101

Notebook PC Applications

Portable Equipment Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 22 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 14 S (typ.)
- Low leakage current: I_{DSS} = −10 μA (max) (V_{DS} = −12 V)
- Enhancement model: V_{th} = −0.5 to −1.2 V
  (V_{DS} = −10 V, I_D = −200 μA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3U1A

Weight: 0.011 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−12	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−12	V
Gate-source voltage		V_{GSS}	±8	V
Drain current	DC (Note 1)	I_D	−6	A
	Pulsed (Note 1)	I_{DP}	−24	
Drain power dissipation (t = 5 s) (Note 2a)		P_D	2.5	W
Drain power dissipation (t = 5 s) (Note 2b)		P_D	0.7	W
Single pulse avalanche energy (Note 3)		E_{AS}	6.3	mJ
Avalanche current		I_{AR}	−3	A
Repetitive avalanche energy (Note 4)		E_{AR}	0.25	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

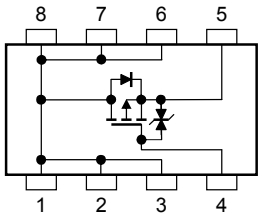
Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 5 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	50.0	°C/W
Thermal resistance, channel to ambient (t = 5 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	178.6	°C/W

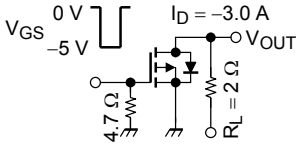
Note: (Note 1), (Note 2), (Note 3), (Note 4) and (Note 5): See the next page.

This transistor is an electrostatic-sensitive device. Please handle with caution.

Circuit Configuration



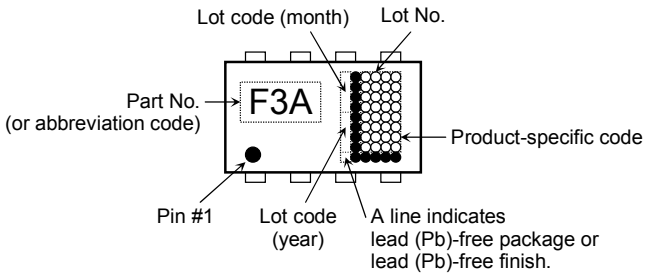
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = −12 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−12	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 8 V	−4	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −200 μA	−0.5	—	−1.2	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −1.8 V, I_D = −1.5 A	—	60	85	mΩ
		$R_{DS\ (ON)}$	V_{GS} = −2.5 V, I_D = −3.0 A	—	32	40	
		$R_{DS\ (ON)}$	V_{GS} = −4.5 V, I_D = −3.0 A	—	22	28	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −3.0 A	7	14	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	1600	—	pF
Reverse transfer capacitance		C_{rss}		—	260	—	
Output capacitance		C_{oss}		—	335	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	7	—	ns
	Turn-on time	t_{on}		—	13	—	
	Fall time	t_f		—	21	—	
	Turn-off time	t_{off}		—	68	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ −10 V, V_{GS} = −5 V, I_D = −6.0 A	—	18.0	—	nC
Gate-source charge		Q_{gs}		—	14.5	—	
Gate-drain (“miller”) charge		Q_{gd}		—	3.5	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

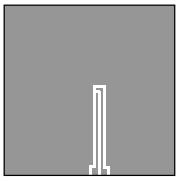
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−24	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −6.0 A, V_{GS} = 0 V	—	—	1.2	V

Marking (Note 5)

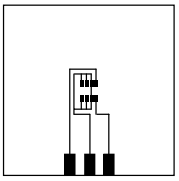


Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



(a)



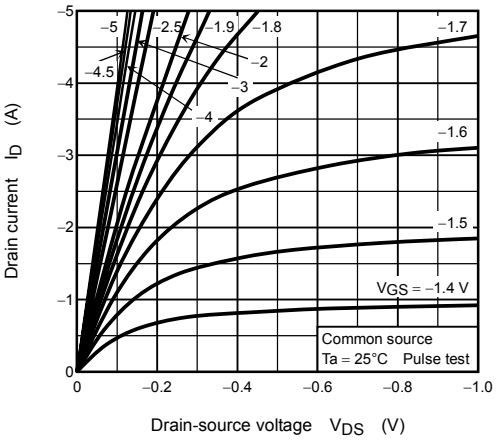
(b)

Note 3: V_{DD} = −10 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = −3.0 A

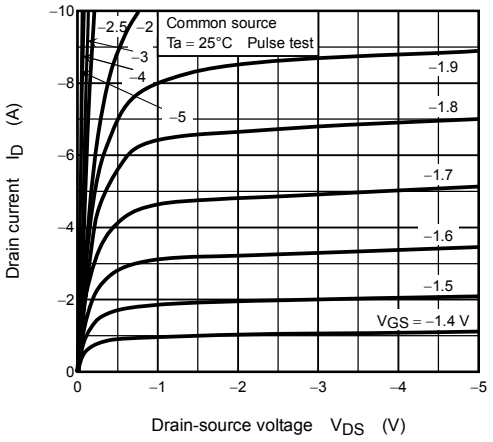
Note 4: Repetitive rating: pulse width limited bymaximum channel temperature

Note 5: A dot on the lower left of the marking indicates Pin 1.

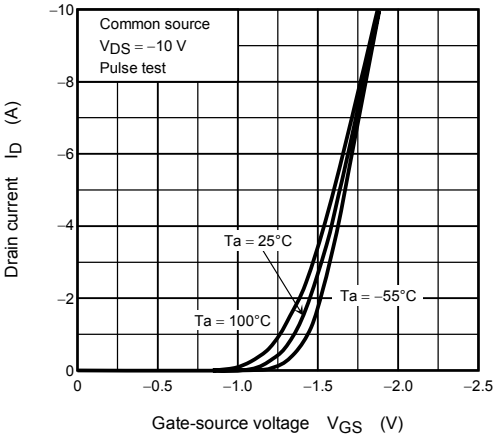
$I_D - V_{DS}$



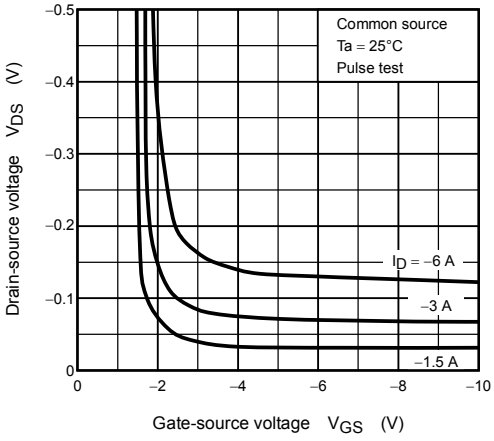
$I_D - V_{DS}$



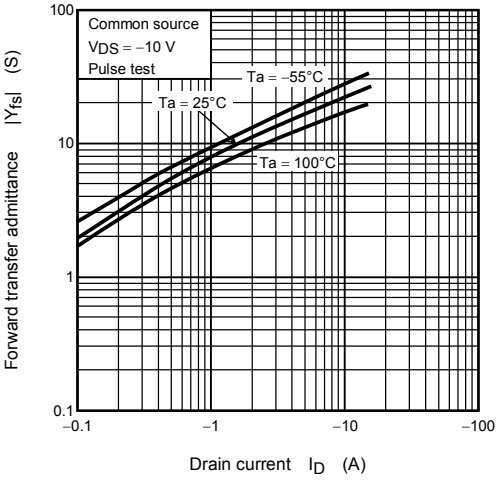
$I_D - V_{GS}$



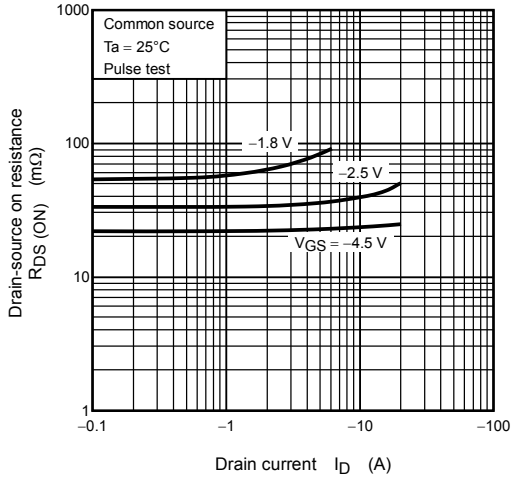
$V_{DS} - V_{GS}$



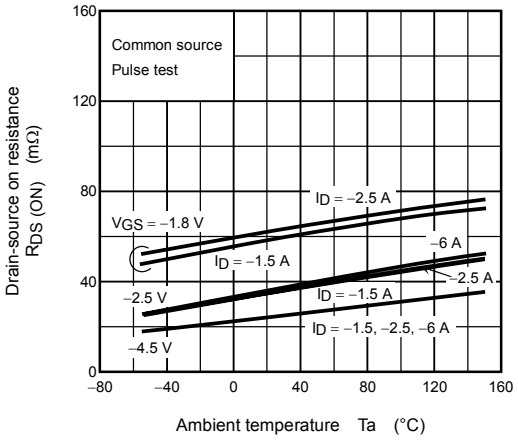
$|Y_{fs}| - I_D$



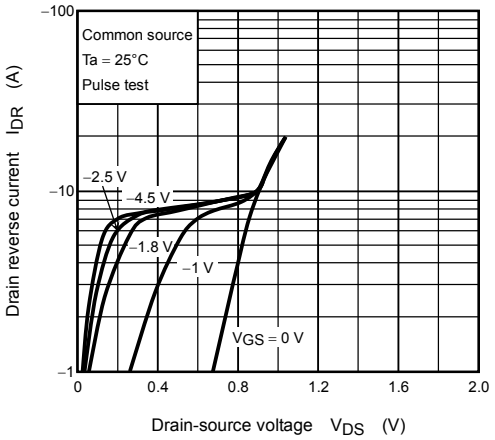
$R_{DS\ (ON)} - I_D$



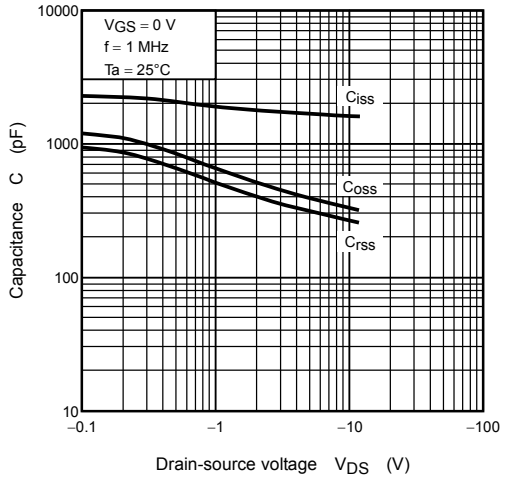
$R_{DS\ (ON)}$ – Ta



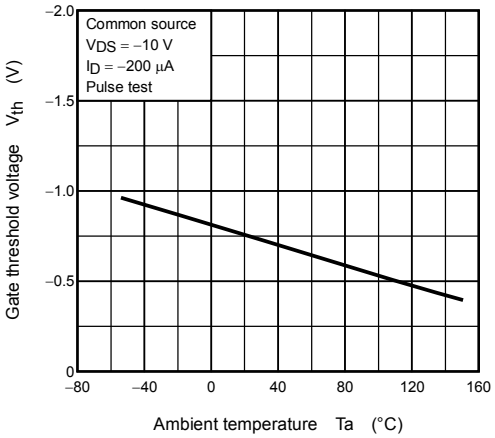
I_{DR} – V_{DS}



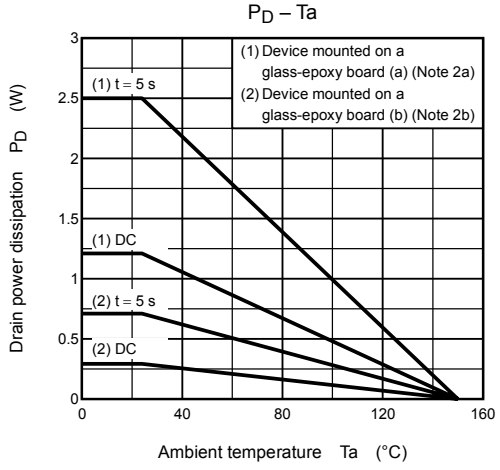
Capacitance – V_{DS}



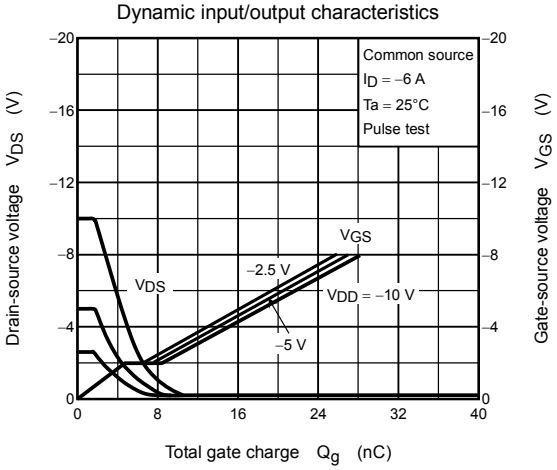
V_{th} – Ta



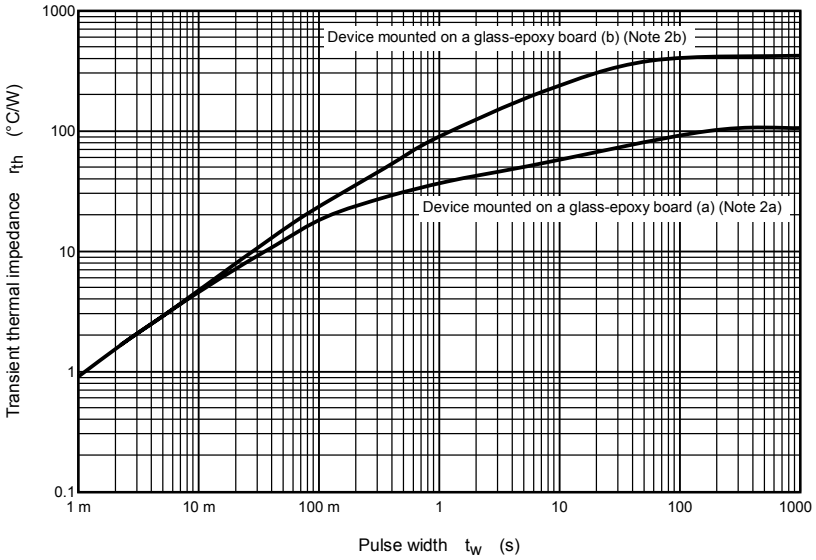
P_D – Ta



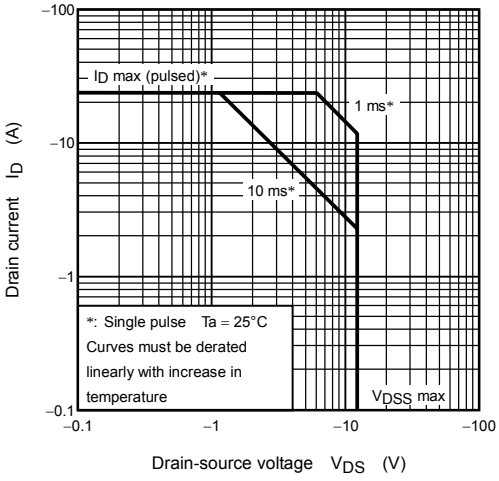
Dynamic input/output characteristics



$r_{th} - t_w$



Safe operating area



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